SYNCHRONOUS MIRROR DELAY (SMD) CIRCUIT AND METHOD INCLUDING A RING OSCILLATOR FOR TIMING COARSE AND FINE DELAY INTERVALS

ABSTRACT OF THE DISCLOSURE

A synchronous mirror delay includes a ring oscillator that generates a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal. In response to an input clock signal, a model delay line generates a model delayed clock signal . having a model delay relative to the input clock signal. A coarse delay circuit generates a coarse delay count responsive to the oscillator, input, and model delayed clock signals, and activates a coarse delay enable signal responsive to the delay count being equal to a reference count value. A fine delay circuit latches the tap clock signals and develops a fine delay from the latched signals, and activates a fine delay enable signal having the fine delay in response to the coarse delay enable signal. An output circuit generates a delayed clock signal responsive to the coarse and fine delay enable signals going active.